REMARKS

The present remarks are in response to the Office Action mailed September 12, 2006, in which Claims 1–4, 6-9 and 15-19 were rejected. Claims 1 and 15 have been amended in this application. No Claims are canceled and no claims are added. Therefore, Claims 1–4, 6-9 and 15-19 remain in this application. In this application, the specification has been amended to add the description of 341 and 342. Thus, the drawings are consistent with the specification and the objection to the drawings is traversed.

Applicants respectfully requests reconsideration in light of the following remarks.

CLAIM REJECTIONS- 35 U.S.C. SECTION 102(e)

Claims 1-4 and 6-9 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2002/0159216 to Ennis.

The Examiner is of the opinion that all features recited in Claims 1-4 and 6-9 are disclosed by Ennis. Ennis provides a vacuum plasma processor with electrode array (202, 204, 206) forming a bottom or top electrode of the plasma processor. In the plasma processor, the electrodes (202, 204, 206) of the array (200) are used as parts of the thermoelectric and parts of the electrostatic chuck to control the localized temperature of the workpieces and the chucking voltage. A circuitry (256, 258, 260) coupled to the electrodes (202, 204, 206) of the array (200) for control one or more localized plasma electric parameter, like voltage, electric current, phase angle and so on, at different location of the workpiece. And the circuitry (256, 258, 260) provides RF power to each electrode of the array with different frequency and power level in order to control the different temperature and the different chucking voltage at different locations

of the workpiece. Besides, the circuitry (256, 258, 260) electrically connect the RF source (240) and each of the electrodes (202, 204, 206) of the array (200), and there is a variable power gain amplifier (250, 252, 254) and a cable (266) between each of the electrodes (202, 204, 206) of the array (200) and the RF source (240). There is a separate matching network (264) between each of the cables (266) and each of the electrodes (202, 204, 206) for matching the voltage, electric current and phase angle output by the amplifier (250, 252, 254), the voltage, electric current and phase angle output by the cables (266), and the predetermined voltage, electric current and phase angle in the plasma process.

The present invention provides a high density plasma chemical vapor deposition equipment with an impedance-matching circuit. The impedance-matching circuit is used to match the inner electrode power output and the outer electrode power output of the bi-polar electrostatic chuck. Thus, the impedance-matching circuit needs to be electrically connected with the inner electrode and the outer electrode. Although the vacuum plasma processor disclosed by Ennis has a separate matching network (264) between each of the electrodes (202, 204, 206) of the array (200) and the RF source (240) and behind the variable power gain amplifier (250, 252, 254) and a cable (266), each of the matching networks (264) are only connected to one electrode (202, 204, 206) of the array (200) for matching the voltage, electric current and phase angle output by the amplifier (250, 252, 254), the voltage, electric current and phase angle output by the cables (266), and the predetermined voltage, electric current and phase angle at each step of the plasma process. The matching networks (264) disclosed by Ennis connects only one electrode, but the impedance-matching circuit of the present invention simultaneously connect both of the inner electrode and the outer electrode of the bi-polar electrostatic chuck. So, the impedance-matching circuit of the present invention can balance the inner electrode power output and the outer electrode power output, but the matching networks (264) disclosed by Ennis can do that because it only connects one electrode. Therefore, the position and the function of the matching networks (264) is different from that of the impedance-matching circuit of the present invention. So, the

impedance-matching circuit of the present invention is not disclosed by Ennis.

Besides, the matching network (264) disclosed by Ennis is used to match the variable power gain amplifier (250, 252, 254) power output, the cables (266) power output, and the power output predetermined in the plasma process at the same circuitry for supply RF power with different frequency and power level to different electrodes. Therefore, Ennis teaches away from the feature of the present invention that the impedance-matching circuit of the present invention simultaneously connects both of the inner electrode and the outer electrode of the bi-polar electrostatic chuck to balance the inner electrode power output and the outer electrode power output. This is because the vacuum plasma processor disclosed by Ennis provide different power to different electrodes of the array to control localized temperature of the workpieces and the chucking voltage. So if the matching network (264) simultaneously connects to two or more electrodes, the vacuum plasma processor disclosed by Ennis cannot provide different power to different electrodes of the array to control localized temperature of the workpieces and the chucking voltage. Therefore, Ennis teaches away from the present invention.

Besides, the impedance matching circuit of the present invention includes a plurality of adjustable inductors, wherein a first terminal of the plurality of adjustable inductors connects to an external circuit and a second terminal of said plurality of adjustable inductors connects to an alternating current bias power; a plurality of adjustable capacitors, wherein a first terminal of the plurality of adjustable capacitors connects to a second terminal of the plurality of inductors and a second terminal of the plurality of adjustable capacitors connects to the ground; a power-measuring device which connects to the second terminal of the plurality of adjustable inductors to measure the power outputs of the second terminal of the plurality of adjustable inductors; a power comparator which connects to the power-measuring device and produces a control signal for automatic impedance regulation; and an automatic impedance-regulator which connects with the plurality of adjustable inductors, the plurality of adjustable capacitors, and the power

comparator, wherein the automatic impedance-regulator receives the control signal for automatic impedance regulation to regulate the impedance values of the plurality of adjustable inductors and the impedance values of the plurality of adjustable capacitors. However, the matching network (264) disclosed by Ennis does not disclose the plurality of adjustable inductors and the plurality of adjustable capacitors of the impedance matching circuit of the present invention, and Ennis does not disclose the connecting relationship between all elements of the impedance matching circuit of the present invention. Therefore, the present invention is not disclosed and taught by Ennis.

According to the above analysis, the amended Claim 1 is not disclosed and taught by Ennis. Therefore, the rejection of Claim 1 is traversed and the rejection of Claims 2-3 and 6-9 is traversed because of their dependency.

CLAIM REJECTIONS- 35 U.S.C. SECTION 103(a)

Claims 15-19 stand rejected under 35 U.S.C. 103(a) as being anticipated over Ennis in view of U.S. Patent 5,535,333 to Castro et al.

The Examiner is of the opinion that the combination of the Ennis and the Castro et al teach all features recited in Claims 15-19.

Castro et al. provides negative offset bipolar electrostatic chuck which can provide the same potential between the two poles of the bipolar electrostatic chuck when the plasma is close d to a wafer hold by the bipolar electrostatic chuck. The bipolar electrostatic chuck system includes a negative-offset power supply for providing a positive potential level to the positive

pole of the bipolar electrostatic chuck and a negative potential level to the negative pole of the bipolar electrostatic chuck. The positive potential level is positively biased relative to a common reference voltage level by a first magnitude while the negative potential level is negatively biased relative to the same common reference voltage level by a second magnitude, which is larger than the first magnitude. The negative-offset power supply provides different potential to the positive pole and the negative pole of the bipolar electrostatic chuck to be an offset before the plasma is closed. When the plasma is closed to the wafer, the offset will balance the potential of the positive pole and the negative pole of the bipolar electrostatic chuck. So the bipolar electrostatic chuck can hold the wafer tightly when the plasma is closed to the wafer.

According to the above interpretation under "**CLAIM REJECTIONS- 35 U.S.C. SECTION 102(e)**", Ennis can not disclose and teach the present invention because the separate matching network (264) only connects one electrode, but not multiple electrodes. And Ennis teaches away from the present invention because the vacuum plasma processor disclosed by Ennis need to provide different power to different electrodes of the array to control localized temperature of the workpieces and the chucking voltage. Therefore, amended Claims 1 and 15 are not disclosed and taught by Ennis. However, Castro et al. does not disclose and teach this feature recited in amended Claims 1 and 15. Thus, amended Claims 1 and 15 are not disclosed and taught by Ennis and Castro et al., and the rejection of Claim 15 is traversed. The rejection of Claims 16-19 is traversed because of their dependency.

Conclusion

In light of the above amendments and remarks, Applicant respectfully submits that all pending Claims 1-4, 6-9 and 15-19 as currently amended are in condition for allowance. Accordingly, reconsideration is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby

made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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